Let your application determine the right microprocessor supervisor

There are a series of steps to follow when implementing a processor-supervisor circuit. Follow them, and you'll be sure to make the right choice.

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Choosing an appropriate microprocessor-supervisor IC from among the hundreds of models available can be a quite a task. The selection process consists of the following five steps:

- Selecting the reset-threshold voltage.
- Selecting the reset time.
- Selecting output characteristics.
- Selecting additional features—manual reset, watchdog, power fail, battery management, multiple voltages, power sequencing, package, and supply current.
- Refining your selection—price and preferred parts.

A supervisor IC keeps the processor in reset mode until the power-supply voltages and clock signals settle down. When you turn on a piece of electronic equipment, the filter capacitors begin to charge, causing the supply voltage to begin ramping up. A phase-locked loop (PLL) (if used to generate the clock signal) starts searching for a phase lock. Because power-supply voltages and clock frequencies are out of spec during this time, digital circuitry may operate erratically. Circuits may turn on at the wrong time, memories may be overwritten, equipment may be damaged, or the system may assume an unrecoverable state.

A voltage monitor (basically a comparator and voltage reference) can assist the supervisor by detecting when the supply voltage is within spec. Unfortunately, supply voltages often fluctuate at turn-on, rising to a satisfactory value for a few milliseconds, then dropping out of spec. Similarly, PLLs may not settle down until many milliseconds after the supply voltages stabilize. Supervisors therefore introduce a delay at the voltage monitor's output before issuing a power-on reset command. If the delay is long enough to allow voltages and frequencies to stabilize, then all the power-on problems can be avoided.

Selecting the reset-threshold voltage

The first step in selecting a supervisor is to determine the voltage at which it starts its delay timer (reset-threshold voltage). Two philosophies govern the selection of this voltage.

The first philosophy is to choose a threshold voltage high enough to guarantee that everything works when the reset is released. This approach precludes any chance of a system startup with supply voltages out of spec, but you must ensure that the minimum supply voltage is above the maximum reset voltage. Because the resulting system is more susceptible to noise and power-supply glitches, this approach is more appropriate for higher-end systems, which tightly control the supply voltages while minimizing glitches and noise.

The second approach is to choose an arbitrarily low threshold voltage. Make sure that the supply voltages finish ramping up and the clocks settle out before the reset timeout ends. This approach tolerates a greater amount of noise and power-supply glitches but includes a risk that the reset will release while supply

voltages are out of spec and that the reset may not occur if supply voltages aren't given sufficient time to fall below the reset threshold when power is cycled on and off. This scheme can also let a processor operate prior to reset below the range of voltages for which its operation is guaranteed. This second approach is therefore appropriate for lower-cost systems in which power-supply regulation, glitches, and noise aren't as tightly controlled.

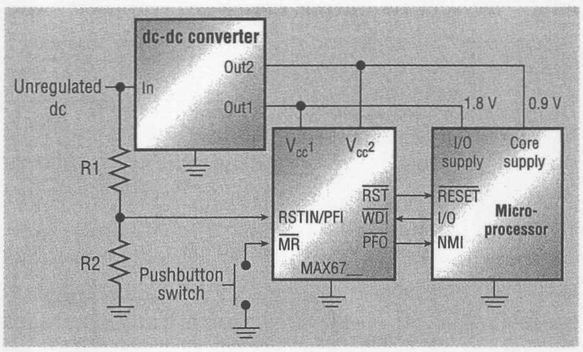
After deciding on a threshold voltage, you still have several decisions to make, such as whether you want a fixed or adjustable threshold. An adjustable threshold reduces stocking requirements and allows easy design modifications, but parts with that feature need more pins and require external components. Thus, an adjustable-voltage part makes sense for low-volume projects and a fixed-voltage part is better for high-volume projects.

The second step in selecting a supervisor is to determine the time interval (reset delay) between the supply voltage reaching its threshold value and the supervisor output telling the processor that it's okay to start processing. This delay must be long enough to allow the supply voltages and clock to stabilize.

Selecting output characteristics

The third step is selecting the output logic. Parts come with either active-high or active-low outputs, and your choice depends on the system requirements. You also need to choose the output type, of which the two most common are open-drain and push-pull. Open-drain outputs allow several devices to be connected together with one pull-up resistor, implementing a "wired-OR" function. That arrangement gives you free logic at the expense of an external resistor. Push-pull outputs, which require no external resistor, are the preferred choice if you don't need the wired-OR function.

Bidirectional is a third, less common output type required by the Motorola 68HC11 and similar processors. It lets the processor determine whether the reset was asserted by an external device or by the processor itself.



1. In a typical application circuit, a multi-voltage supervisor ensures that a microcontroller operates properly.

Selecting additional features

The fourth step in selecting a supervisor is determining what additional features you require. Supervisors with a manual reset input let you reset the processor independent of the voltage-monitor function. This input can be connected to a pushbutton on the front panel or to internal logic. Make sure you include ESD protection if the manual reset signal originates off the card! Manual reset is useful for debugging and final testing as well as for products that are never powered down.

When pressed once, most pushbutton switches bounce on and off several times in rapid succession—a behavior that can cause problems in a digital system. As a result, most manual reset inputs come "debounced" to ensure that the supervisor issues just one reset each time the button is pressed. If your application doesn't include a pushbutton switch, the manual reset input can instead be used to wire-OR other logic signals with the reset function. Some manual reset functions include a one-shot circuit to ensure repeatable resets. Other manual reset inputs require that the input be held for a longer period before asserting, making them useful for front-panel applications.

Occasionally, a microprocessor gets lost and deviates from normal code execution due to an aberration such as a programming error, voltage glitch, or stray cosmic ray. Watchdog circuits detect such faults and reset the system to a known state. To implement a watchdog circuit, the processor must be set up to supply periodic interrupts, which reset the timer before it has a chance to time out. If the processor gets lost and doesn't generate an interrupt on schedule, the watchdog times out and resets the system.

When designing a watchdog system, you must select a processor-interrupt period and watchdog-timeout interval. The interrupt period should be as long as practical because it consumes processor overhead. The minimum watchdog interval must be longer than the maximum interrupt period.

Some "windowed watchdogs" monitor the watchdog input for signals that occur too fast or too slow. In addition, some pin-selectable parts let you adjust the watchdog timing by setting a few logic inputs. To avoid inadvertent resets during a long startup time (i.e., when the processor is first powered up), many watchdog timers can be disabled or made subject to a startup delay.

When a system loses power, it's nice to have advance notice that lets the system initiate a power-down routine and save critical parameters in memory. A typical system might have an unregulated dc input and an inter-

nal dc-dc converter for generating the system power. Let's assume a 5-V input that's converted to 3.3 V. When the 5-V supply is interrupted, energy stored in the power-supply input capacitors remains. Thus, the input voltage decays as the input capacitors discharge, but the dc-dc converter maintains the 3.3-V output in regulation until the input voltage approaches 3.3 V.

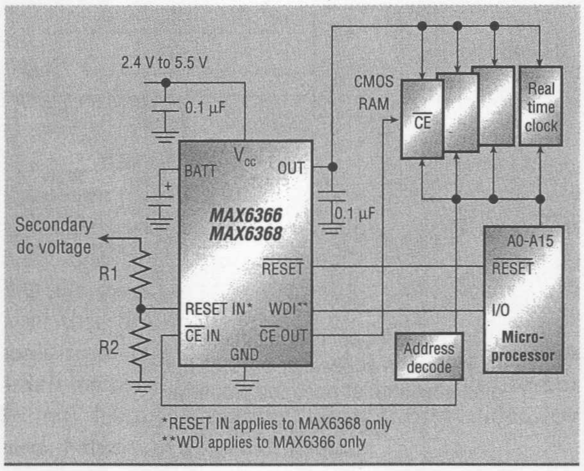
A power-fail comparator at the input can give advance notice of such an impending power failure. The amount of notice depends on the filter capacitors' size and their discharge rate (current drawn). Putting the system in low-power mode as soon as it detects a power failure can increase the amount of time available.

If you don't have access to the input power or you want to save a pin, choose a supervisor with a low-line output. That function monitors the power-supply output instead of its input. A low-line output circuit is similar to the power-on reset, but with a higher voltage threshold and no delay on the output. It may be easier to implement but won't give as much notice of an impending power loss as does a power-fail comparator circuit (*see Fig. 1*).

Many systems include components such as real time clocks and volatile memories, which must be powered constantly to avoid loss of critical information. Such systems require some form of battery backup that can switch between the main and battery power. Use a simple diode-OR circuit to draw power automatically from whichever input voltage is highest, but the voltage drop across the diode can cause a substantial efficiency loss.

Often, the battery voltage is so close to the system's minimum operating voltage that the use of a diode and its associated voltage drop isn't practical. In that case, a transistor switch is needed. The switch should be controlled by circuitry that monitors the main power-supply voltage and switches to battery backup when the main power drops below a threshold value.

With battery-powered systems, you tend to get an abundance of advance notice on battery failure by monitoring the battery voltage. A low-battery detector indicates when battery capacity has declined to a level that's low yet still adequate to power the device. Its output can warn the user to replace the batteries or to put the system in a low-power mode.



2. In addition to the reset, watchdog timer, and chip-enable gating functions, this device employs a backup battery to maintain memory contents in the event of failure in the main supply.

Chip-enable gating prevents the writing of erroneous data during an under-voltage condition by disabling the memory devices. The chip-enable for a memory device passes through the supervisor. It passes through unaltered during normal operation, but during reset, the supervisor forces chip-enable high. That action protects the memory contents by disabling the chip and preventing writes to memory. A supervisor IC that includes a typical battery-backup circuit switches to the backup battery to ensure data is maintained in memory after the main power source has failed (*see Fig. 2*).

Another feature to consider for products that include battery backup is the battery freshness seal. When a product includes a non-rechargeable battery as backup power source, you want to ensure that the battery is fresh when it reaches the customer. A supervisor IC without this feature will switch the load over to the battery whenever the main power supply is unavailable—an action guaranteed to occur at any time between the product's manufacture and first actual use.

The battery freshness seal for a supervisor ensures that the battery and load remain disconnected even when no main supply voltage is present. The IC remains in this mode until the user applies power for the first time. This special mode is initiated during testing by forcing an output line to ground (often chip-enable out). The scheme ensures this mode is not triggered during normal operation.

Modern systems often have multiple power supplies, and you may not want to allow the processor to come out of reset until all the supply voltages are within spec. A multiple-input-voltage reset can reduce the number of parts required to monitor all the supply voltages.

Multiple supplies often need to be brought up in a particular sequence, or portions of a system need to be enabled in a particular order. Multiple supervisors set up as delay generators have performed this function in the past, but newer parts combine the multiple delays in one device. PD

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